Express Mail Label No.: EL 844 515 165 US

ATTORNEY'S DOCKET NO.: S1022/8827

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Cesare CLEMENTI, Gabriella GHIDINI, and Carlo RIVA
Serial No.:	Unassigned
Filing Date:	Herewith
For:	PROCESS FOR FORMING AN INTEGRATED CIRCUIT COMPRISING NON-VOLATILE MEMORY CELLS AND SIDE TRANSISTORS OF AT LEAST TWO DIFFERENT TYPES, AND CORRESPONDING IC
Examiner:	Unassigned
Art Unit:	Unassigned

Box Patent Application
Commissioner for Patents
Washington, D.C. 20231

Sir:

PRELIMINARY AMENDMENT

IN THE SPECIFICATION

Please replace the paragraph beginning at line 14 of page 6 as shown.

FIGS. 1a-1f show diagrammatic cross section views of successive steps of a process for the formation of non-volatile memory cells and peripheral transistors of a first and a second type in accordance with the present invention.

Please replace the paragraph beginning at line 19 of page 6 as shown.

The description of a formation process for memory cells and peripheral transistors in accordance with the present invention is given below with reference to one preferred embodiment of the present invention as shown in FIGS. 1a-1f. These figures show unscaled diagrammatic cross section views and illustrate in successive steps a formation process for a non-volatile memory cell and at least first and second peripheral MOS transistors. The partial structures of the cell and the transistors are indicated respectively by reference numbers 1, 2

and 3. The regions R1, R2 and R3 represent the zones in which are formed the cell 1 and the transistors 2 and 3.

Please replace the paragraph beginning at line 19 of page 10 as shown.

After the above described formation of the intermediate dielectric multilayer of the cell and the gate dielectric of the peripheral transistors, completion of the cell and the transistors takes place through standard process steps. In particular a second polysilicon layer, or poly 2, and if desired a silicide layer are deposited and then patterned for the simultaneous formation of the control gate 12 of the cell and of the gate of the transistors, as shown in FIG. 1f. The process is completed by appropriate implantations, formation of a passivation layer and of the interconnections by means of opening of contacts, and deposition of one or more metallization layers.

IN THE DRAWINGS

Applicants enclose 1 sheet of Informal Drawings showing a new Figure 1F. Approval is requested.

IN THE CLAIMS

Please cancel claims 2 and 9 without prejudice or disclaimer.

Please amend claims 1, 3, 4, 5, 6 and 7 as follows:

Applicant presents the claims as amended below and encloses a separate sheet indicating the amendments to the claims with bracketing and underlining.

1. (Amended) An integrated circuit on a monocrystalline substrate, the integrated circuit comprising:

a matrix of non-volatile memory cells, each non-volatile memory cell having a floating gate and a control gate, both gates being electroconductive, and an intermediate dielectric

multilayer disposed between the floating gate and the control gate for electrically insulating the floating gate and the control gate from one another, the intermediate dielectric multilayer including at least a first deposited silicon oxide layer; and

at least one first and one second transistor type formed in zones of the substrate peripheral to the matrix of non-volatile memory cells and having multilayer gate dielectrics of a first and second thickness, respectively, wherein the multilayer gate dielectric of both the first type and the second type of peripheral transistors includes a second silicon oxide layer formed by means of a thermal treatment, and the first deposited silicon oxide layer overlying the second silicon oxide layer, the first deposited silicon oxide layer being densified by said thermal treatment that forms the second silicon oxide layer.

3. (Amended) The integrated circuit of claim 1, wherein said transistors of the first and the second type are high voltage and low voltage transistors, respectively, and said second thickness of the multilayer gate dielectric of the second transistor type is less than said first thickness of the multilayer gate dielectric of the first transistor type.

4. (Amended) The integrated circuit of claim 1, wherein a thickness of said multilayer gate dielectric of said second transistor type is less than that of said multilayer gate dielectric of said first transistor type.

5. (Amended) The integrated circuit of claim 1, wherein at least one of the multilayer gate dielectrics of the first and second types are nitridized to increase the quality and reliability of the gate dielectrics.

6. (Amended) The integrated circuit of claim 1, wherein a thickness of said first deposited silicon oxide layer is between 50Å and 250Å and said first thickness and said second thickness of the multilayer gate dielectrics of the at least one first and one second transistor types are between 70Å and 350Å.

7. (Amended) An integrated circuit comprising:

a substrate;

at least one memory cell formed in the substrate, the memory cell having a floating gate, a control gate, and a multilayer dielectric disposed between the floating gate and the control gate and including a deposited layer, the multilayer dielectric insulating the floating gate from the control gate; and

first and second transistors formed in the substrate in an area of the substrate peripheral to the at least one memory cell, each transistor having a gate dielectric comprising:

the deposited layer; and

a first layer underlying the deposited layer of the first transistor, formed by thermal oxidation of the substrate which also acts to densify the deposited layer.

Please add the following new claims:

10. The integrated circuit of claim 7, wherein the first transistor includes a second layer between the deposited layer and the first layer, the second layer being formed by thermal oxidation of the substrate.

11. The integrated circuit of claim 1, wherein the multilayer gate dielectric of the first transistor type includes a third silicon oxide layer formed between the first deposited layer and the second silicon oxide layer by thermal oxidation and wherein the thermal treatment that forms the second silicon oxide layer is thermal oxidation.

REMARKS

This is a preliminary amendment in which claims 2 and 9 have been canceled and claims 10-11 have been added to further define Applicants' contribution to the art. An early and favorable action is hereby earnestly solicited.

Respectfully submitted,

Cesare CLEMENTI, Gabriella GHIDINI, and Carlo RIVA

By: _____

James H. Morris
Registration No.: 34,681
Wolf, Greenfield & Sacks, P.C.
600 Atlantic Avenue
Federal Reserve Plaza
Boston, MA 02210
Tel. No. (617) 720-3500
Attorneys for Applicants

Attorney Docket No. S1022/8827
Dated: January 14, 2002

MARKED UP CLAIMS

1. (Amended) An integrated circuit on a monocrystalline substrate, the integrated circuit comprising:

a matrix of non-volatile memory cells, each non-volatile [floating] memory cell having a floating gate and a control gate, both gates being electroconductive, and an intermediate dielectric multilayer disposed between the floating gate and the control gate for electrically insulating the floating gate and the control gate from one another, the intermediate dielectric multilayer including at least a first deposited silicon oxide layer; and

at least one first and one second transistor type formed in zones of the substrate peripheral to the matrix of non-volatile memory cells and having multilayer gate dielectrics of a first and second thickness, respectively, wherein the multilayer gate dielectric of both the first type and the second type of peripheral transistors includes a second silicon oxide layer formed by means of a thermal treatment, and [a third] the first deposited silicon oxide layer overlying the second silicon oxide layer, the [third] first deposited silicon oxide layer being densified by said thermal treatment that forms the second silicon oxide layer.

3. (Amended) The integrated circuit of claim 1, wherein said transistors of the first and the second type are high voltage and low voltage transistors, respectively, and said second thickness of the multilayer gate dielectric of the second transistor type is less than said first thickness of the multilayer gate dielectric of the first transistor type.

4. (Amended) The integrated circuit of claim 1, wherein [the] a thickness of said multilayer gate dielectric of said second transistor type is less than that of said multilayer gate dielectric of said first transistor type.

5. (Amended) The integrated circuit of claim 1, wherein at least one of the multilayer gate dielectrics of the first and second types are nitridized to increase the quality and reliability of the gate dielectrics.

6. (Amended) The integrated circuit of claim 1, wherein [the] a thickness of said first deposited silicon oxide layer is between 50Å and 250Å and said first thickness and said second thickness of the multilayer gate dielectrics of the at least one first and one second transistor types are between 70Å and 350Å.

7. (Amended) An integrated circuit comprising:

a substrate;

at least one memory cell formed in the substrate, the memory cell having a floating gate, a control gate, and a multilayer dielectric disposed [on] between the floating gate and the control gate and including a deposited layer, the multilayer dielectric insulating the floating gate from the control gate; and

[a] first and second transistors formed in the substrate in an [first] area of the substrate peripheral to the at least one memory cell, [the first] each transistor having a gate dielectric comprising:

the deposited layer; and

a first layer underlying the deposited layer of the first transistor, formed by thermal oxidation of the substrate which also acts to densify the deposited layer.[; and

a second layer underlying the deposited layer of the first transistor, formed by thermal oxidation of the substrate; and

a second transistor formed in the substrate in a second area of the substrate peripheral to the at least one memory cell, the second transistor having a gate dielectric comprising:

the deposited layer; and

a first layer underlying the deposited layer of the second transistor, formed by thermal oxidation of the substrate.]

MARKED-UP SPECIFICATION

Please replace the paragraph beginning at line 14 of page 6 as shown.

FIGS. 1a-1f [e] show diagrammatic cross section views of successive steps of a process for the formation of non-volatile memory cells and peripheral transistors of a first and a second type in accordance with the present invention.

Please replace the paragraph beginning at line 19 of page 6 as shown.

The description of a formation process for memory cells and peripheral transistors in accordance with the present invention is given below with reference to one preferred embodiment of the present invention as shown in FIGS. 1a-1f [e]. These figures show unscaled diagrammatic cross section views and illustrate in successive steps a formation process for a non-volatile memory cell and at least first and second peripheral MOS transistors. The partial structures of the cell and the transistors are indicated respectively by reference numbers 1, 2 and 3. The regions R1, R2 and R3 represent the zones in which are formed the cell 1 and the transistors 2 and 3.

Please replace the paragraph beginning at line 19 of page 10 as shown.

After the above described formation of the intermediate dielectric multilayer of the cell and the gate dielectric of the peripheral transistors, completion of the cell and the transistors takes place through standard process steps. In particular a second polysilicon layer, or poly 2, and if desired a silicide layer are deposited and then patterned for the simultaneous formation of the control gate 12 of the cell and of the gate of the transistors, as shown in FIG. 1f. The process

is completed by appropriate implantations, formation of a passivation layer and of the interconnections by means of opening of contacts, and deposition of one or more metallization layers.